We claim:

1. A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

receiving a signal; and

synchronization hunting concurrently for a first and second frame alignment pattern for a first and second alignment candidates.

2. The machine-readable medium of claim 1 wherein the first and second alignment candidates are stored in a set of per-alignment state machines.

3. The machine-readable medium of claim 1 wherein the first frame alignment pattern for the first alignment candidate coincides with the second frame alignment pattern for the second alignment candidate.

4. The machine-readable medium of claim 1 further comprising:

receiving a second signal simultaneously with the signal; and

synchronization hunting concurrently for the first and second frame alignment pattern for a third and fourth alignment candidates of the second signal.

5. The machine-readable medium of claim 1 further comprising:

receiving a second signal simultaneously with the signal, the second signal being a different format than the signal; and

synchronization hunting the second signal.

6. A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

receiving a bit stream;

storing a set of bits of the bit stream in a set of per-alignment state machines; and

hunting for a first frame alignment bit pattern for a first one of the set of per-alignment state machines in concurrence with hunting for a second frame alignment bit pattern for a second one of the set of per-alignment state machines.

7. The machine-readable medium of claim 6 wherein the first frame alignment bit pattern for the first one of the set of per-alignment state machines coincides with the second frame alignment bit pattern for the second one of the set of per-alignment state machines.

8. The machine-readable medium of claim 6 further comprising:

receiving a second bit stream simultaneously with the bit stream;

initializing the set of per-alignment state machines; and

hunting concurrently for the first and second frame alignment bit pattern for the first and second one of the set of per-alignment state machines.

9. The machine-readable medium of claim 6 further comprising:

receiving a second bit stream simultaneously with the bit stream, the second bit stream being a different format than the bit stream;

initializing the set of per-alignment state machines; and

hunting the second signal for a third frame alignment pattern.

10. A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

receiving a first and second signal;

initializing a set of per-alignment state machines;

hunting for a first alignment signal within the first signal in a first time slice;

resetting the set of per-alignment state machines after the first time slice; and

hunting for a second alignment signal within the second signal in a second time slice.

11. The machine-readable medium of claim 10 wherein the first alignment signal coincides with a third alignment signal for a first and second one of the per-alignment state machines.

12. The machine-readable medium of claim 10 wherein the second alignment signal coincides with a fourth alignment signal for a first and second one of the per-alignment state machines.

13. The machine-readable medium of claim 10 further comprising:

hunting for a third alignment signal within the first signal in concurrence with the hunting for the first alignment signal in the first signal in the first time slice; and

hunting for the third alignment signal within the second signal in concurrence with the hunting for the second alignment signal within the second signal in a second time slice.

14. The machine-readable medium of claim 10 further comprising:

hunting for a third alignment signal within the first signal in concurrence with the hunting for the first alignment signal in the first signal in the first time slice; and

hunting for a fourth alignment signal within the second signal in concurrence with the hunting for the second alignment signal within the second signal in a second time slice.

15. A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

receiving a first and second signal;

initializing a set of per-alignment state machines;

hunting for a first alignment signal in the first signal for a first one of the set of per-alignment state machines in concurrence with hunting for a second alignment signal in the first signal for a second one of the set of per-alignment state machines in a first time slice;

resetting the set of per-alignment state machines after the first time slice; and

hunting for a third alignment signal in the second signal for a third one of the set of per-alignment state machines in concurrence with hunting for a fourth alignment signal in the second signal for a fourth one of the set of per-alignment state machines in a second time slice.

16. The machine-readable medium of claim 15 wherein the first and second alignment signals coincide for the first and second one of the set of per-alignment state machines and the first and second alignment signal coincide for the third and fourth one of the set of per-alignment state machines.

17. The machine-readable medium of claim 15 wherein the first and second signal have the same formatting.

18. The machine-readable medium of claim 15 wherein the first and second signal have different formatting.

19. A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

sync hunting for a first layer format of a signal;

finding alignment of the signal for the first layer format; and

resetting sync hunting for a second layer format of the signal in response to finding alignment of the signal for the first layer format.

20. The machine-readable medium of claim 19 further comprising:

resetting sync hunting for the first layer format for a second signal;

sync hunting for the first layer format of the second signal;

finding alignment of the second signal for the first layer format; and

resetting sync hunting for the second layer format of the second signal in response to finding alignment of the second signal for the first layer format.

21. The machine-readable medium of claim 19 further comprising:

resetting sync hunting for the first layer format for a second signal;

sync hunting for the first layer format of the second signal;

finding alignment of the second signal for the first layer format; and

resetting sync hunting for a third layer format of the second signal in response to finding alignment of the second signal for the first layer format.

22. The machine-readable medium of claim 19 further comprising:

resetting sync hunting for a third layer format for a second signal;

sync hunting for the third layer format of the second signal;

finding alignment of the second signal for the third layer format; and

resetting sync hunting for a fourth layer format of the second signal in response to finding alignment of the second signal for the third layer format.

23. An apparatus comprising:

a domain clock to transmit a clock signal;

a first and second receiving unit coupled to the domain clock, the first and second receiving unit to receive a first and second signal;

a selecting unit coupled to the first and second receiving unit, the selecting unit to synchronize the first and second signal with the clock signal and cycle between transmitting the first and second signal as a third signal;

a first memory unit coupled to the selecting unit, the first memory unit to receive the second signal and store a set of counters and a global state machine;

a second memory unit coupled to the first memory unit, the second memory unit to store a set of per-alignment state machines; and

a sync hunting logic coupled to the selecting unit, first memory unit and second memory unit, the sync hunting logic to sync hunt the third signal with the set of per-alignment state machines, global state machines, and the set of counters and to feed a set of output to the first and second memory unit.

24. The apparatus of claim 23 wherein the first and second signals have different formats.

25. The apparatus of claim 23 wherein the first and second signals are received at different rates.

26. The apparatus of claim 23 wherein the second signal is a set of signals.

27. The apparatus of claim 23 wherein the domain clock outruns a combined rate of the first and second signal.

28. The apparatus of claim 23 wherein the sync hunt logic sync hunts a first and second frame alignment pattern concurrently.

29. An apparatus comprising:

a set of parallel registers to store a set of bits from a signal;

a set of counters coupled to the set of parallel registers, the counters to count the set of bits;

a first memory unit coupled to the set of parallel registers and the set of counters, the first memory unit to store a global state machine;

a second memory unit coupled to the first storage, the second memory unit to store a set of per-alignment state machines; and

a sync hunt logic coupled to the set of parallel registers, the first memory unit, and the second memory unit, the sync hunt logic to sync hunt the signal in a clock domain with the set of per-alignment state machines and the global state machine, and feed a set of information to the first and second memory unit.

30. The apparatus of claim 29 wherein the sync hunt logic concurrently hunts for a first and second frame alignment pattern in the signal for a first and second one of the set of per-alignment state machines.

31. The apparatus of claim 29 wherein a rate of the clock domain is faster than a rate of the signal.

32. The apparatus of claim 29 further comprising:

a first and second receiving unit , the first and second receiving unit to receive a first and second signal and synchronize the first and second signal in the clock domain; and

a multiplexing unit coupled to the set of parallel registers and the first and second receiving unit, the multiplexing unit to multiplex the first and second signal and transmit the multiplexed first and second signal as the signal to the set of parallel registers.

33. An apparatus comprising:

a first set of registers to store a set of bits of a signal;

a per-channel state memory coupled to the first set of registers, the per-channel state memory to store a set of counters and a global state machine;

a sync hunt per-alignment memory coupled to the set of registers and the per-channel state memory, the sync hunt per-alignment memory to store a set of per-alignment state machines;

a second set of registers coupled to the per-channel state memory, sync hunt per-alignment memory and the first set of registers, the second set of registers to store a second set of bits received from the first set of registers, the per-channel state memory, and the sync hunt per-alignment memory; and

a sync hunt logic coupled to the second set of registers, the sync hunt logic to sync hunt a first and second signal in a clock domain and feed a third set of bits into the per-channel state memory and the sync hunt per-alignment memory.

34. The apparatus of claim 33 wherein the sync hunt logic concurrently hunts for a first and second frame alignment pattern in the signal for a first and second one of the set of per-alignment state machines.

35. The apparatus of claim 33 wherein a rate of the clock domain is faster than a rate of the signal.

36. The apparatus of claim 33 further comprising:

a first and second receiving unit , the first and second receiving unit to receive a first and second signal and synchronize the first and second signal in the clock domain; and

a multiplexing unit coupled to the first set of registers and the first and second receiving unit, the multiplexing unit to multiplex the first and second signal and transmit the multiplexed first and second signal as the signal to the first set of registers.

37. An apparatus comprising:

a receiving unit to receive a signal;

a first memory unit coupled to the receiving unit, the first memory unit to store a set of counters and a global state machine;

a second memory unit coupled to the receiving unit and the first memory unit, the second memory unit to store a set of per-alignment state machines; and

a sync hunt logic coupled to the receiving unit, first memory unit and second memory unit, the sync hunt logic to concurrently hunt for a first and second framing signal in the signal and feed a set of information to the first and second memory unit.

38. The apparatus of claim 37 wherein the signal is a multiplexed signal.

39. The apparatus of claim 37 wherein the first and second framing signal coincide for a first one and second one of the set of per-alignment state machines.

40. The apparatus of claim 37 wherein a first one and second one of the set of per-alignment state machines are accessible simultaneously.

41. The apparatus of claim 37 further comprising:

a domain clock to transmit a clock signal; and

a second receiving unit coupled to the domain clock and the receiving unit, the second receiving unit to receive a second and third signal, to synchronize the second and third signal to the clock signal, and to cycle with the clock signal between transmitting the second and third signal to the receiving unit.

42. An apparatus comprising:

a domain clock to transmit a clock signal;

a receiving unit coupled to the domain clock, the receiving unit to receive a first and second signal and cycle between transmitting the first and second signal as a third signal in accordance with the clock signal;

a first memory unit coupled to the receiving unit, the first memory unit to store a set of counters and a global state machine;

a second memory unit coupled to the receiving unit and the first memory unit, the second memory unit to store a set of per-alignment state machines; and

a sync hunt logic coupled to the receiving unit, first memory unit and second memory unit, the sync hunt logic to concurrently hunt for a first and second framing signal of the third signal.

43. The apparatus of claim 42 wherein a first one and second one of the set of per-alignment state machines are accessible simultaneously.

44. The apparatus of claim 42 wherein the first and second framing signal coincide for a first one and second one of the set of per-alignment state machines.

45. The apparatus of claim 42 wherein the domain clock runs at a rate faster than a combined rate of the first and second signal.

46. An apparatus comprising:

a domain clock to transmit a clock signal;

a first receiving unit coupled to the domain clock, the first receiving unit to receive a first signal and to synchronize the signal to the clock signal;

a second receiving unit coupled to the domain clock, the second receiving unit to receive a second signal and to synchronize the second signal to the clock signal;

a first memory unit coupled to the first receiving unit, the first memory unit to store a first set of counters and a first global state machine;

a second memory unit coupled to the first memory unit, the second memory unit to store a first set of per-alignment state machines;

a first sync hunt logic coupled to the first and second memory unit and the first receiving unit, the first sync hunt logic to sync hunt the first signal and feed an output to the first and second memory unit;

a multiplexing unit coupled to the first and second receiving unit, the multiplexing unit to multiplex the first and second signal in accordance with the clock signal;

a third memory unit coupled to the multiplexing unit and the first sync hunt logic, the third memory unit to store a second set of counters and a second global state machine;

a fourth memory unit coupled to the third memory unit, the fourth memory unit to store a second set of per-alignment state machines; and

a second sync hunt logic coupled to the multiplexing unit and third and fourth memory unit, the second sync hunt logic to sync hunt the multiplexed first and second signal and feed an output to the third and fourth memory unit.

47. The apparatus of claim 46 wherein the first set of per-alignment state machines is organized for simultaneous accessibility of a first and second one of the first set of per-alignment state machines.

48. The apparatus of claim 46 wherein the second set of per-alignment state machines is organized for simultaneous accessibility of a first and second one of the second set of per-alignment state machines.

49. The apparatus of claim 46 wherein the first sync hunt logic concurrently hunts for a first and second frame alignment pattern for a first and second one of the first set of per-alignment state machines.

50. The apparatus of claim 46 wherein the second sync hunt logic concurrently hunts for a first and second frame alignment pattern for a first and second one of the second set of per-alignment state machines.

51. The apparatus of claim 46 further comprising:

the first sync hunt logic to transmit a feed forward signal to the second global state machine when the first sync hunt logic determines alignment for the first signal; and

the second global state machine to reset the second set of per-alignment state machines in response to the feed forward signal.

52. An apparatus comprising:

a first format sync hunt logic to sync hunt a signal for a first layer format and transmit a feed forward signal when the first layer format is determined for the signal;

a global state machine coupled to the first format sync hunt logic, the global state machine to reset a second layer format sync hunt logic in response to the feed forward signal; and

the second format sync hunt logic coupled to the global state machine and the first format sync hunt logic; the second format sync hunt logic to sync hunt the signal for a second layer format.

53. The apparatus of claim 52 wherein the first format sync hunt logic hunts concurrently for a first and second framing pattern of the first layer format.

54. The apparatus of claim 52 further comprising:

a domain clock to transmit a clock signal;

a first and second receiving unit coupled to the domain clock, the first and second receiving unit to receive a second and third signal and to synchronize the second and third signal in accordance with the clock signal; and

a multiplexing unit coupled to the first format sync hunt logic and the first and second receiving unit, the multiplexing unit to multiplex the second and third signal and transmit the multiplexed second and third signal as the signal to the first format sync hunt logic.

55. An apparatus comprising:

a data structure to store a set of DS3 per-alignment state machines, the per-alignment state machines organized into two columns of eighty-five DS3 per-alignment state machines;

a logic coupled to the data structure, the logic to process the set of DS3 per-alignment state machines and to update the set of DS3 per-alignment state machines.

56. The apparatus of claim 55 further comprising a global state machine coupled to the data structure, the global state machine to control the set of DS3 per-alignment state machines.

57. An apparatus comprising:

a data structure to store a set of DS2 per-alignment state machines, the per-alignment state machines organized into three columns of forty-nine DS2 per-alignment state machines;

a logic coupled to the data structure, the logic to process the set of DS-2 per-alignment state machines.

58. The apparatus of claim 57 further comprising a global state machine coupled to the data structure, the global state machine to control the set of DS2 per-alignment state machines.

59. A computer implemented method comprising:

receiving a signal; and

synchronization hunting concurrently for a first and second frame alignment pattern for a first and second alignment candidates.

60. The computer implemented method of claim 59 wherein the first and second alignment candidates are stored in a set of per-alignment state machines.

61. The computer implemented method of claim 59 wherein the first frame alignment pattern for the first alignment candidate coincides with the second frame alignment pattern for the second alignment candidate.

62. The computer implemented method of claim 59 further comprising:
receiving a second signal simultaneously with the signal; and
synchronization hunting concurrently for the first and second frame alignment pattern for a third and fourth alignment candidates of the second signal.

63. The computer implemented method of claim 59 further comprising:
receiving a second signal simultaneously with the signal, the second signal being a different format than the signal; and
synchronization hunting the second signal.

64. A computer implemented method comprising:
receiving a first and second signal;
initializing a set of per-alignment state machines;
hunting for a first alignment signal within the first signal in a first time slice;
resetting the set of per-alignment state machines after the first time slice; and
hunting for a second alignment signal within the second signal in a second time slice.

65. The computer implemented method of claim 64 wherein the first alignment signal coincides with a third alignment signal for a first and second one of the per-alignment state machines.

66. The computer implemented method of claim 64 wherein the second alignment signal coincides with a fourth alignment signal for a first and second one of the per-alignment state machines.

67. The computer implemented method of claim 64 further comprising:

hunting for a third alignment signal within the first signal in concurrence with the hunting for the first alignment signal in the first signal in the first time slice; and

hunting for the third alignment signal within the second signal in concurrence with the hunting for the second alignment signal within the second signal in a second time slice.

68. The computer implemented method of claim 64 further comprising:

hunting for a third alignment signal within the first signal in concurrence with the hunting for the first alignment signal in the first signal in the first time slice; and

hunting for a fourth alignment signal within the second signal in concurrence with the hunting for the second alignment signal within the second signal in a second time slice.